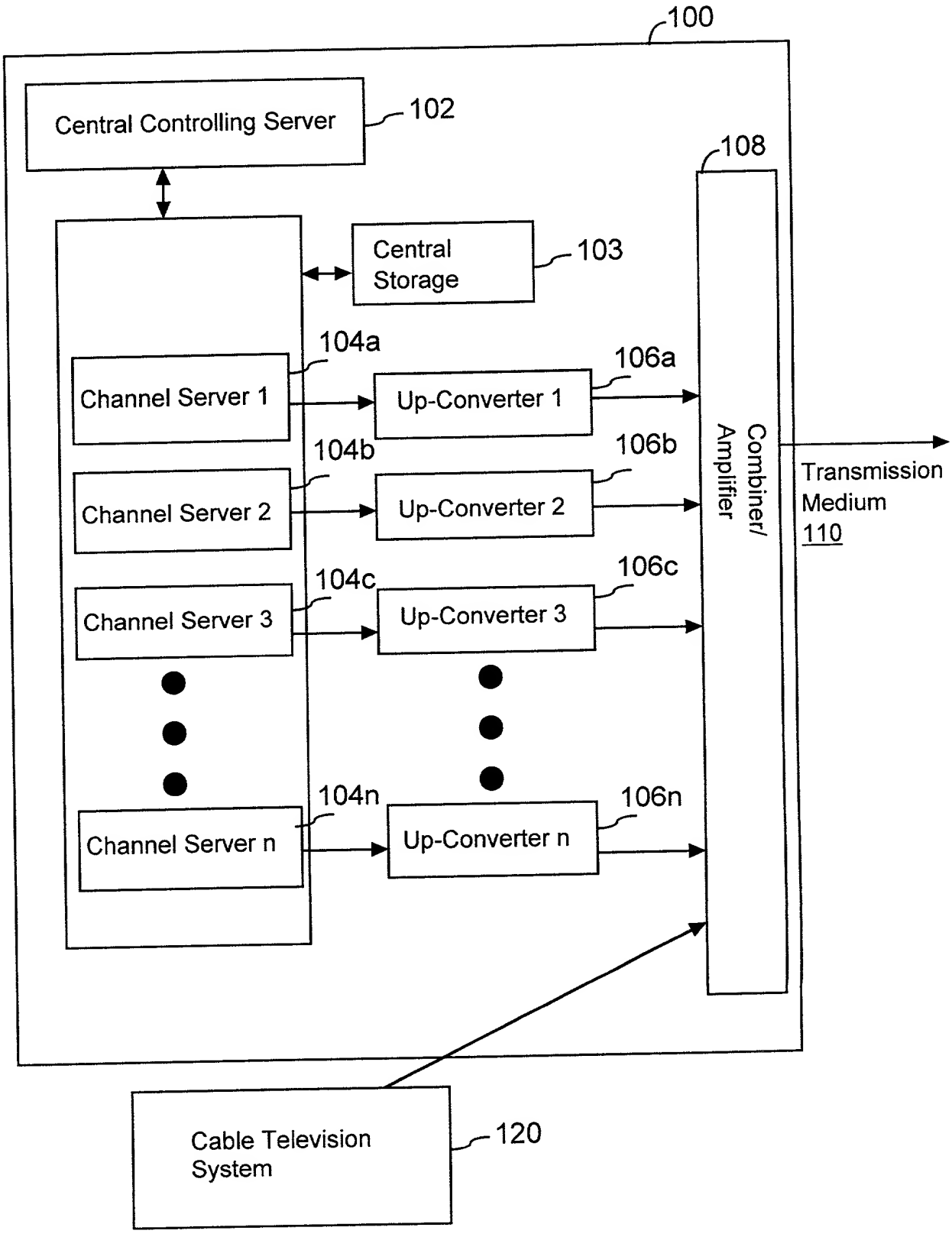
100
Central Controlling Server
102
108
Central Storage
103
104a
Channel Server 1
106a
Up-Converter 1
104b
Channel Server 2
106b
Up-Converter 2
104c
Channel Server 3
106c
Up-Converter 3
104n
Channel Server n
106n
Up-Converter n
Combiner/ Amplifier
Transmission Medium
110
Cable Television System
120

FIG. 1A

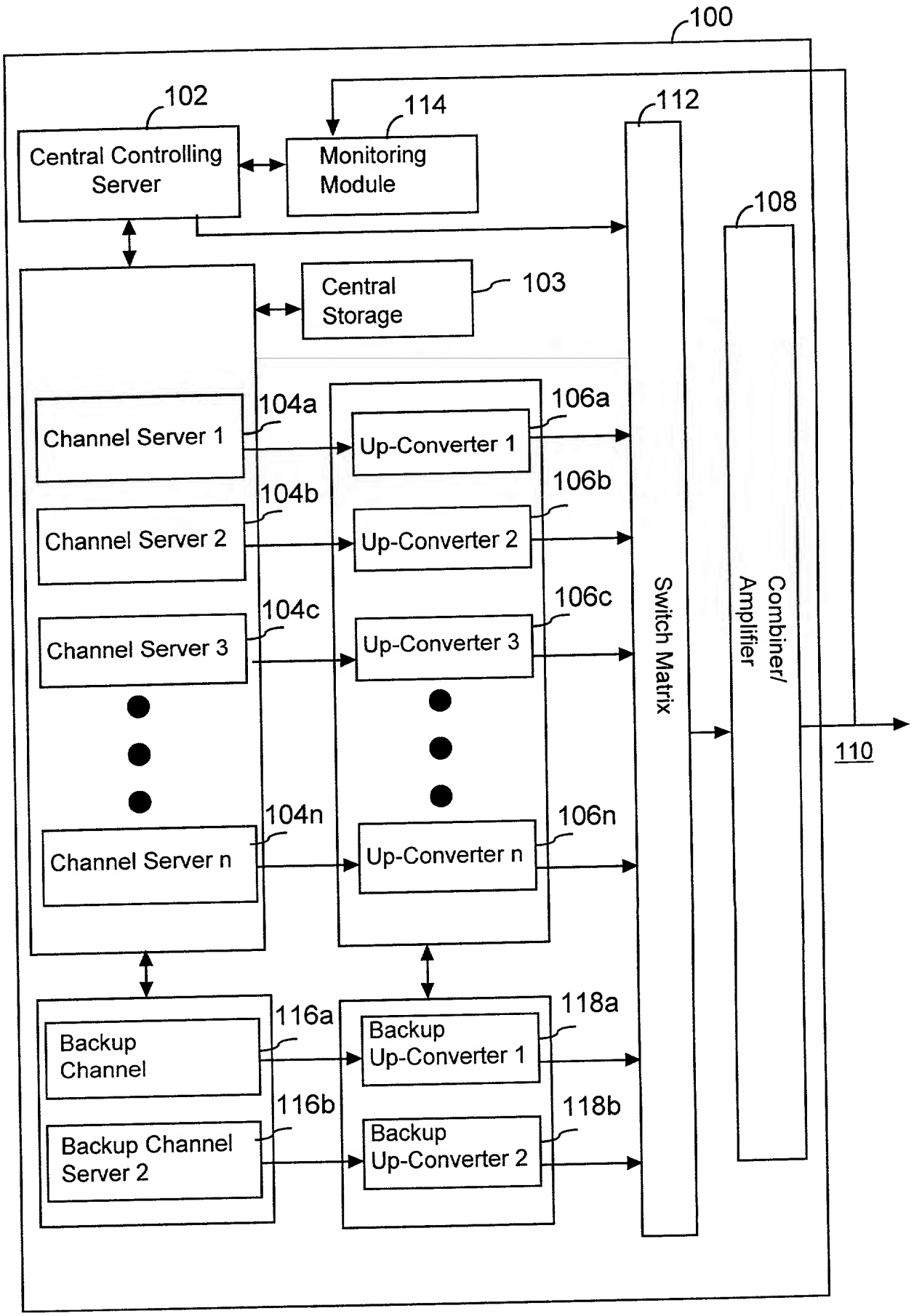
100
102
Central Controlling Server
114
Monitoring Module
112
108
Central Storage
103
Channel Server 1
104a
Up-Converter 1
106a
Channel Server 2
104b
Up-Converter 2
106b
Channel Server 3
104c
Up-Converter 3
106c
Channel Server n
104n
Up-Converter n
106n
Switch Matrix
Combiner/ Amplifier
110
Backup Channel
116a
Backup Up-Converter 1
118a
Backup Channel Server 2
116b
Backup Up-Converter 2
118b

FIG. 1B

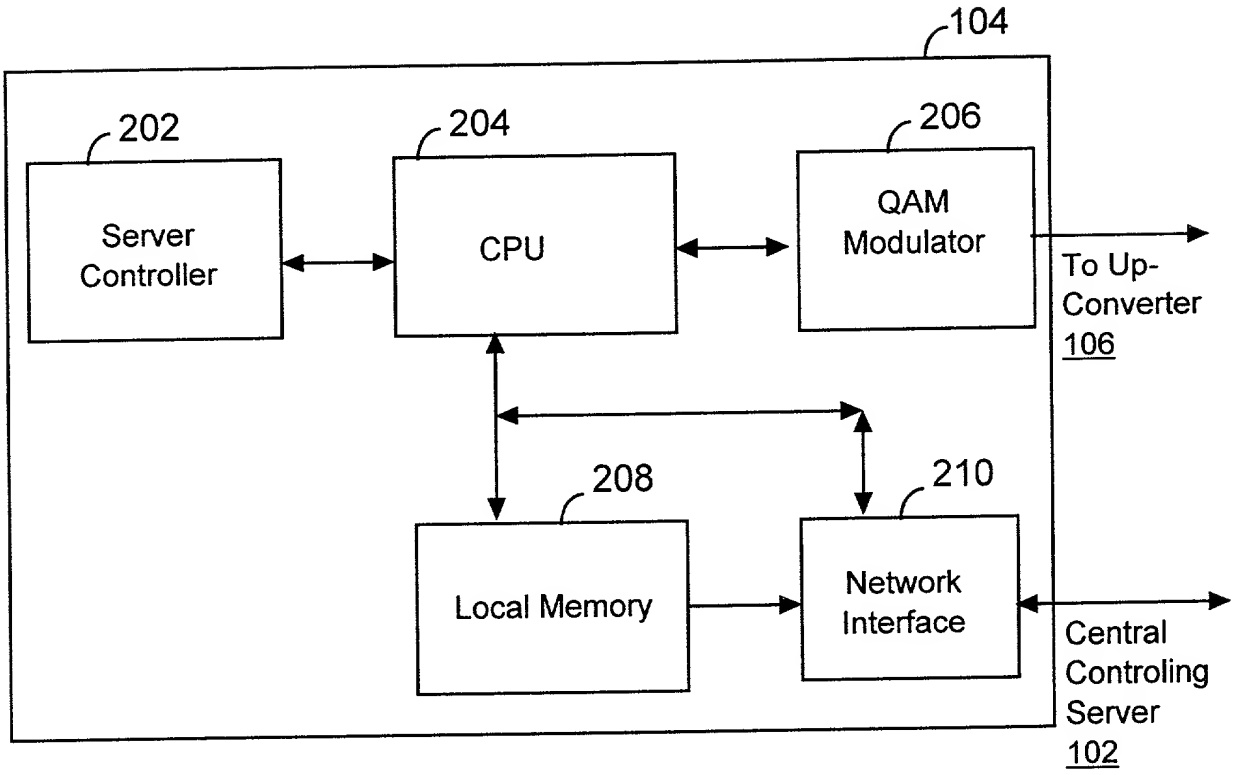
104
202
Server Controller
204
CPU
206
QAM Modulator
To Up-Converter 106
208
Local Memory
210
Network Interface
Central Controling Server 102

FIG. 2

SCANNED,# 10

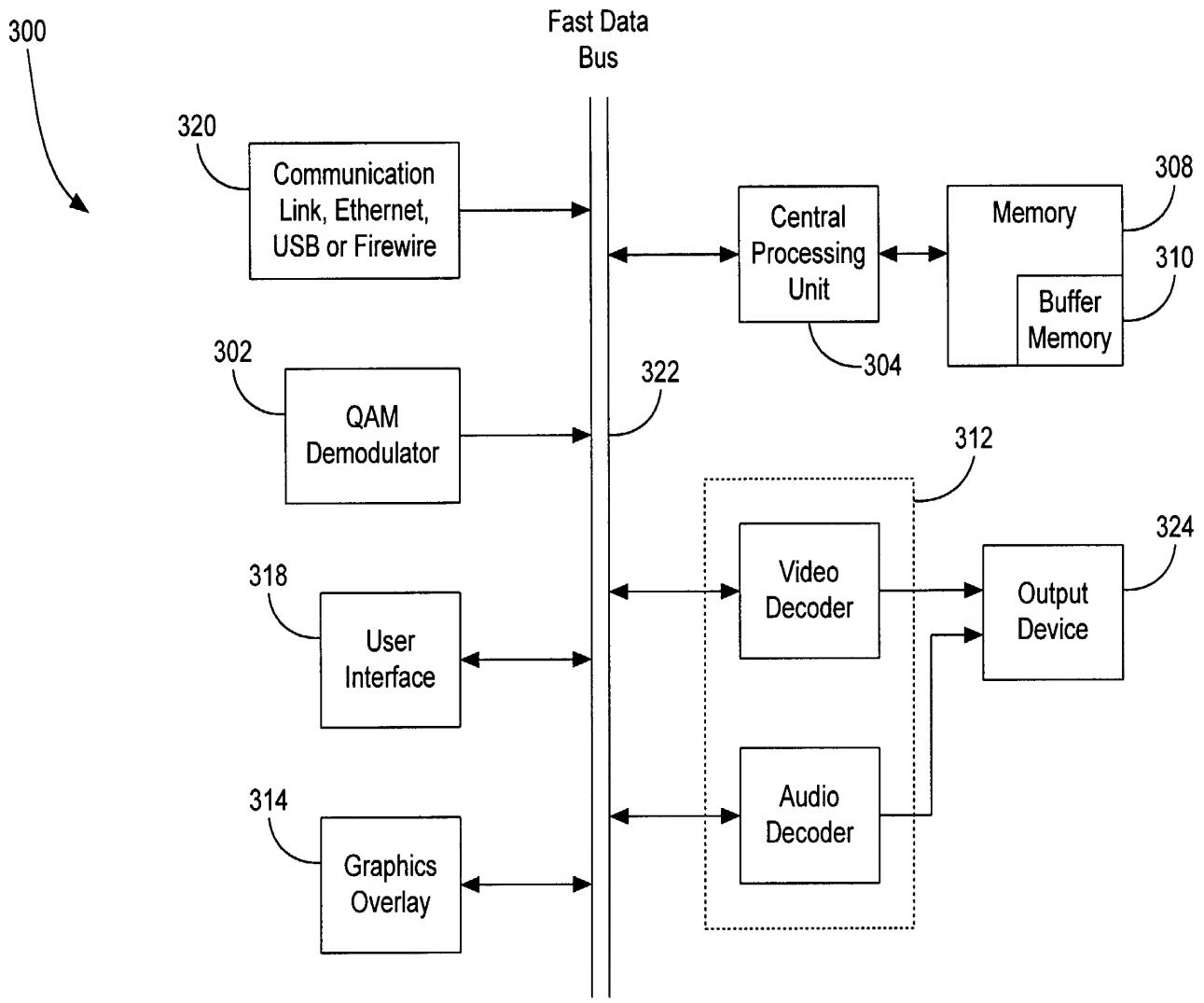

FIG. 3

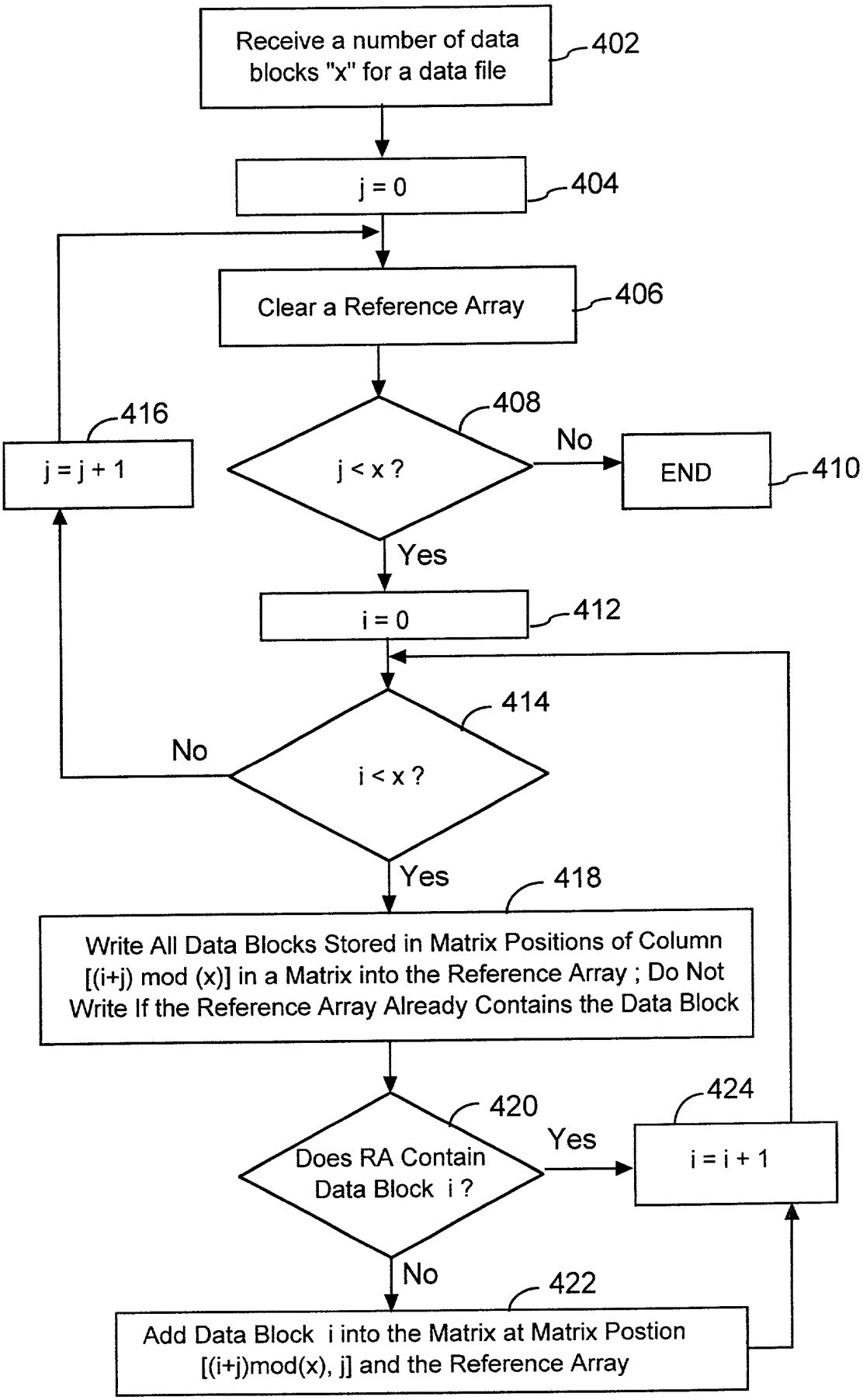
Receive a number of data blocks "x" for a data file
402
j = 0
404
Clear a Reference Array
406
j < x ?
408
No
END
410
Yes
j = j + 1
416
i = 0
412
i < x ?
414
No
Yes
Write All Data Blocks Stored in Matrix Positions of Column [(i+j) mod (x)] in a Matrix into the Reference Array ; Do Not Write If the Reference Array Already Contains the Data Block
418
Does RA Contain Data Block i ?
420
Yes
i = i + 1
424
No
Add Data Block i into the Matrix at Matrix Postion [(i+j)mod(x), j] and the Reference Array
422

FIG. 4

Time Slot	Bandwidth			
TS0	blk0	<-->	<-->	<-->
TS1	blk0	blk1	blk3	<-->
TS2	blk0	blk2	<-->	<-->
TS3	blk0	blk1	blk3	blk4
TS4	blk0	blk4	<-->	<-->
TS5	blk0	blk1	blk2	blk5

FIG. 5

Scheduling Matrix

Time Slot	Bandwidth			
TS0	blk0	blk0	blk1	blk3
TS1	blk0	blk2	blk0	blk1
TS2	blk3	blk4	blk0	blk4
TS3	blk0	blk1	blk2	blk5
TS4				
TS5				

FIG. 6

Scheduling Matrix with Idle Bandwidth Filled

Time Slot	Bandwidth			
TS0	blk0	blk0	blk1	blk3
TS1	blk0	blk2	blk0	blk1
TS2	blk3	blk4	blk0	blk4
TS3	blk0	blk1	blk2	blk5

FIG. 7

New Reduced Idle Bandwidth Scheduling Matrix

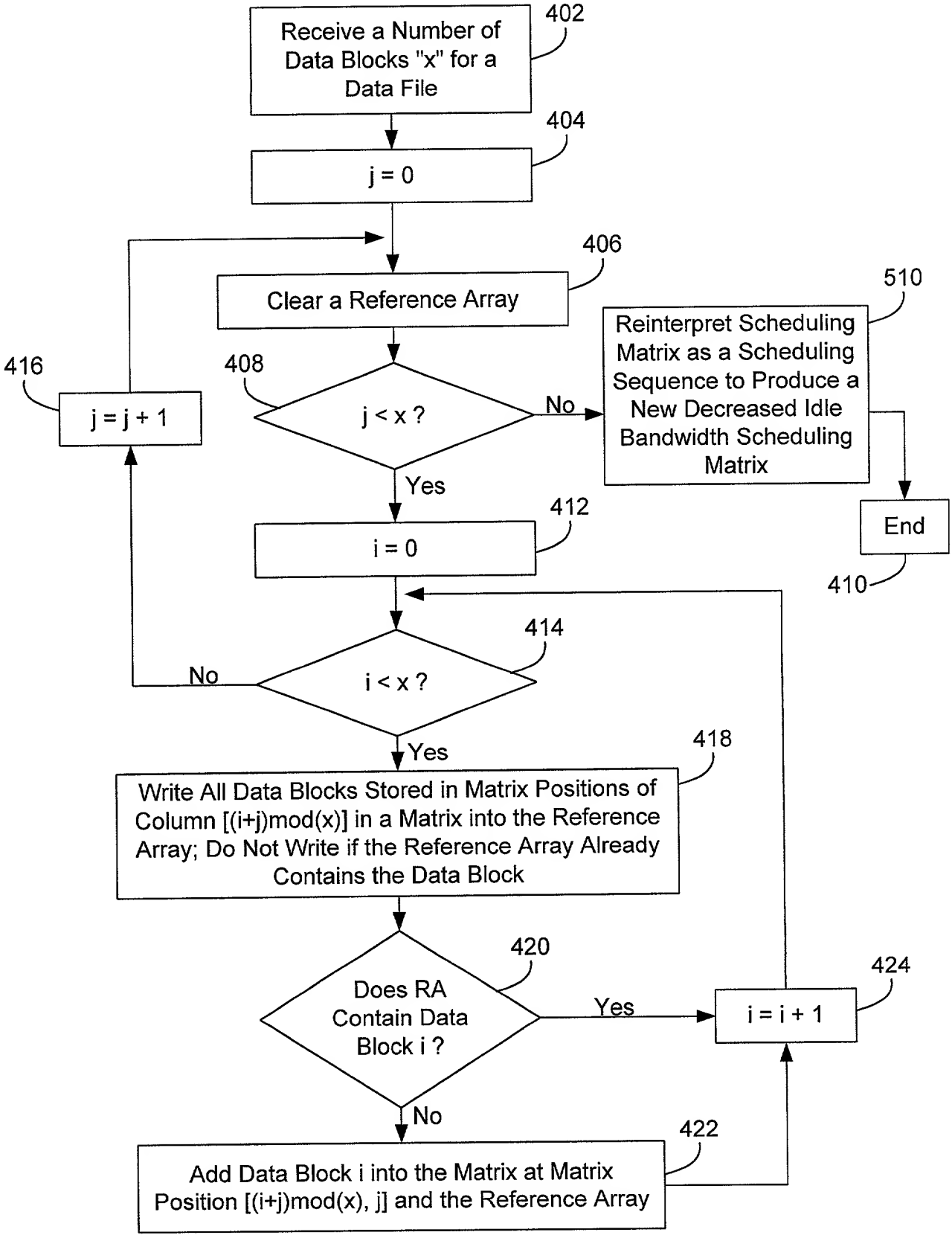
Receive a Number of Data Blocks "x" for a Data File
402
j = 0
404
Clear a Reference Array
406
j < x ?
408
No
Yes
Reinterpret Scheduling Matrix as a Scheduling Sequence to Produce a New Decreased Idle Bandwidth Scheduling Matrix
510
End
410
j = j + 1
416
i = 0
412
i < x ?
414
No
Yes
Write All Data Blocks Stored in Matrix Positions of Column [(i+j)mod(x)] in a Matrix into the Reference Array; Do Not Write if the Reference Array Already Contains the Data Block
418
Does RA Contain Data Block i ?
420
Yes
i = i + 1
424
No
Add Data Block i into the Matrix at Matrix Position [(i+j)mod(x), j] and the Reference Array
422

FIG. 8

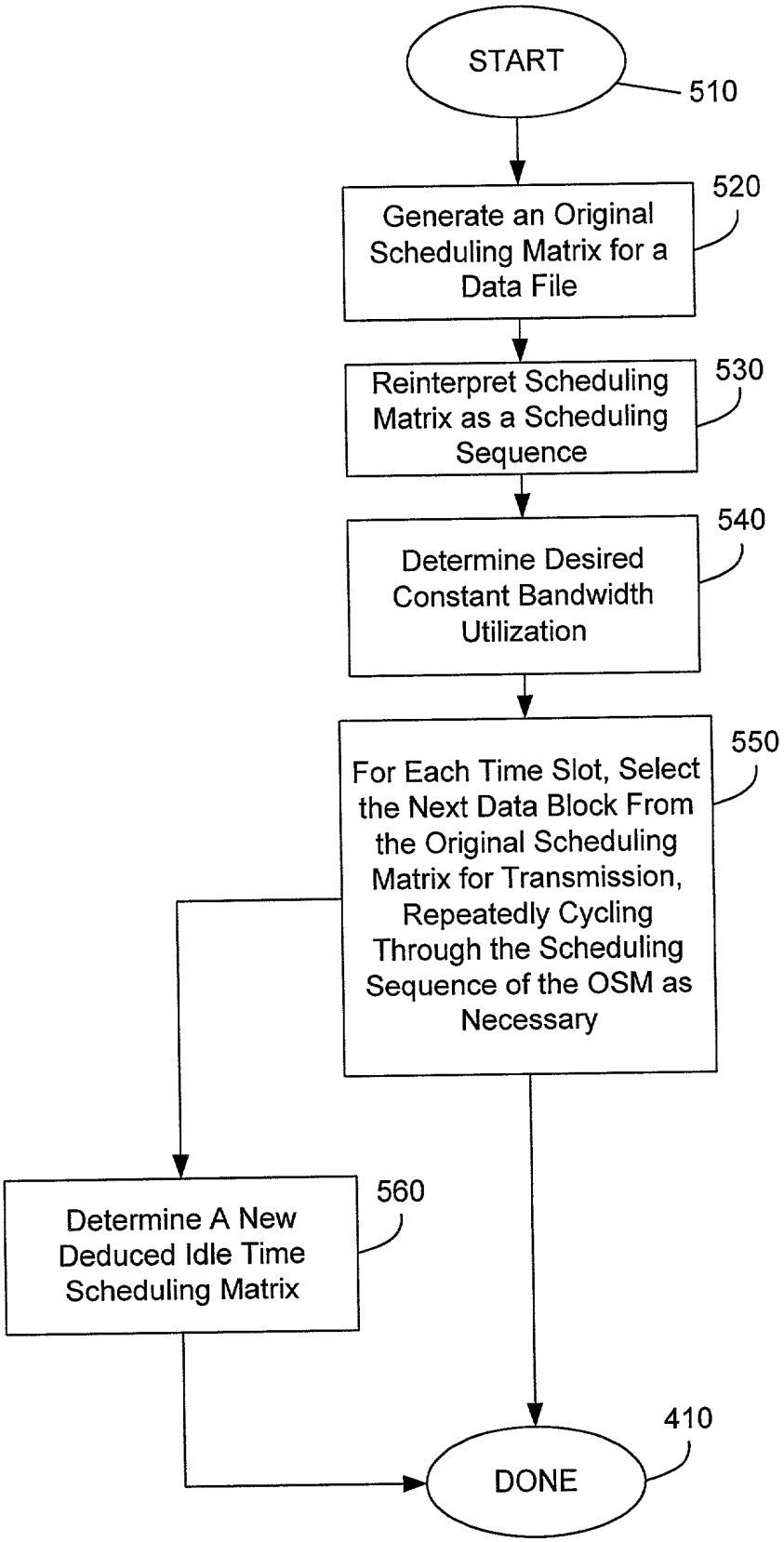
START
510
Generate an Original Scheduling Matrix for a Data File
520
Reinterpret Scheduling Matrix as a Scheduling Sequence
530
Determine Desired Constant Bandwidth Utilization
540
For Each Time Slot, Select the Next Data Block From the Original Scheduling Matrix for Transmission, Repeatedly Cycling Through the Scheduling Sequence of the OSM as Necessary
550
Determine A New Deduced Idle Time Scheduling Matrix
560
DONE
410

FIG. 9

Time Slot	Bandwidth			
TS0	blk0	<-->	<-->	<-->
TS1	blk0	blk1	blk3	<-->
TS2	blk0	blk2	<-->	<-->
TS3	blk0	blk1	blk3	blk4
TS4	blk0	blk4	<-->	<-->
TS5	blk0	blk1	blk2	blk5

570

Time Slot	Bandwidth			
TS0	blk0	blk0	blk1	blk3
TS1	blk0	blk2	blk0	blk1
TS2	blk3	blk4	blk0	blk4
TS3	blk0	blk1	blk2	blk5

575

stream0=> blk0, blk0, blk1, blk3, blk0, blk2, blk0, blk1, blk3, blk4, blk0, blk4, blk0, blk1, blk2, blk5

580

stream0'=> blk1, blk3, blk2, blk1, blk3, blk4, blk4, blk1, blk2, blk5
stream1=> blk0

585

stream0"=> blk2, blk4, blk4, blk2, blk5
stream1=> blk0
stream2=> blk1, blk3, blk1, blk3, blk1

590

FIG. 10